BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

(12) UK Patent Application (19) GB (11) 2 244 374 (13) A

(43) Date of A publication 27.11.1991

(21) Application No 9011399.4

(22) Date of filing 22.05.1990

(71) Applicant
STC plc

(Incorporated in the United Kingdom)

1B Portland Place, London, W1N 3AA, United Kingdom

(72) Inventors
Paul John Rosser
Stephen Robert Jennings
Kevin Bryan Affolter
Kenneth George Snowdon

(74) Agent and/or Address for Service
J P W Ryan
STC Patents, West Road, Harlow, Essex, CM20 2SH,
United Kingdom

(51) INT CL[5]
H01L 21/60

(52) UK CL (Edition K)
H1K KRM K4C11 K4C5M K4F11G K4F18 K4F22D
K4F7A K4F7C K5E2

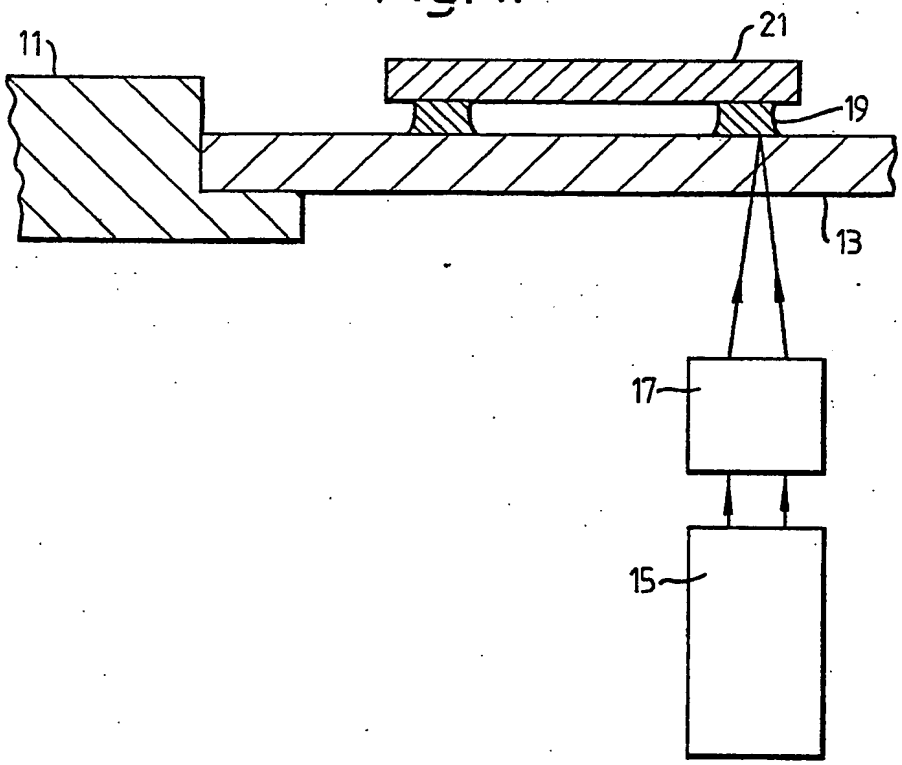
(56) Documents cited
GB 1385112 A GB 1238335 A GB 1162184 A
GB 0991267 A EP 0019186 A1

(58) Field of search
UK CL (Edition K) H1K KLH KRL KRM
INT CL[5] H01L

(54) **Radiation beam bonding of semiconductor device contacts**

(57) Soldered joints 19 in a circuit assembly comprising a semiconductor substrate 13 supporting a plurality of flip chips 21 are fused by directing laser radiation through the substrate wafer on to selected joints. The technique may be employed for the repair of defective solder connections. A carbon divider laser is suitable for use with silicon substrates which are transparent to radiation above 1 micron.

Fig. 1.



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

GB 2 244 374 A

Fig. 1.

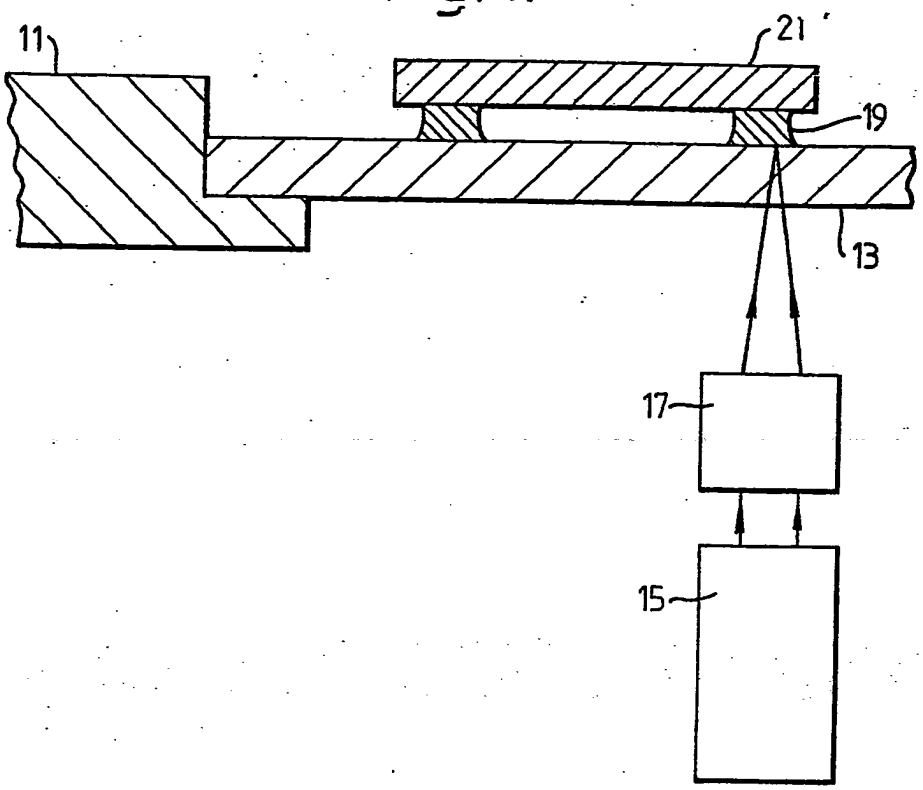
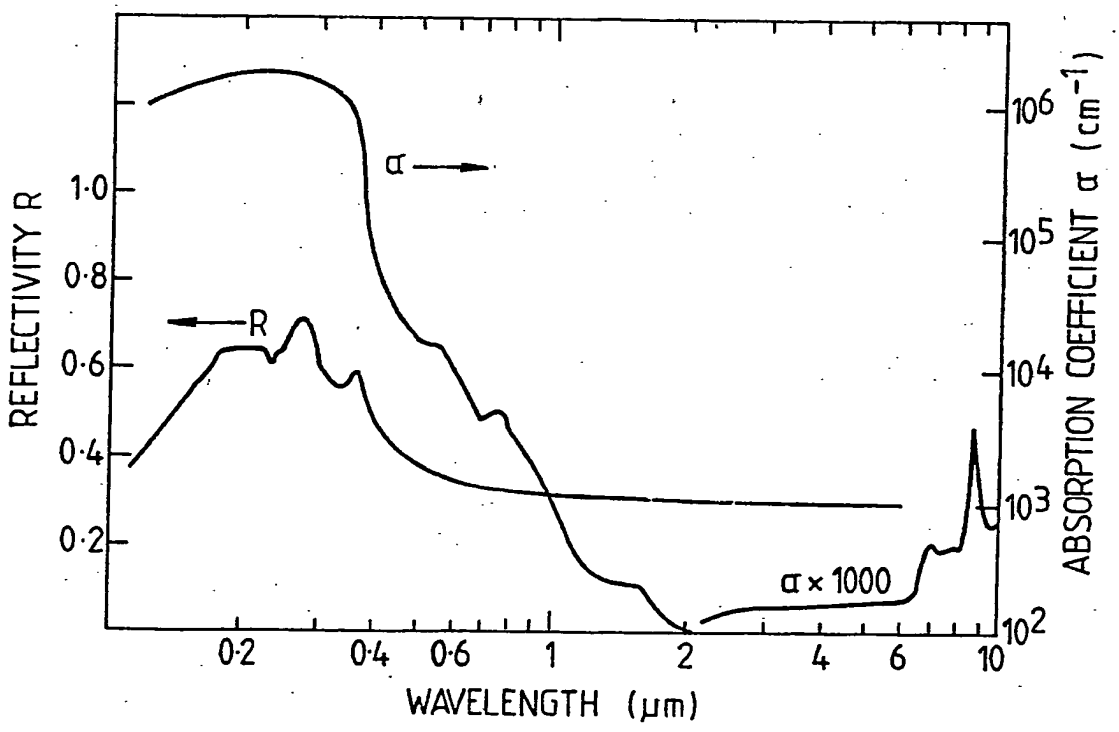

11
21
19
13
17
15

Fig. 2.


REFLECTIVITY R
1·0
0·8
0·6
0·4
0·2
α
R
α × 1000
0·2
0·4
0·6
1
2
4
6
10
WAVELENGTH (μm)
ABSORPTION COEFFICIENT α (cm⁻¹)
10⁶
10⁵
10⁴
10³
10²

IMPROVEMENTS IN HYBRID CIRCUITS

This invention relates to hybrid circuits, and in particular to hybrid circuit constructions of integrated circuit chips supported on a semiconductor wafer substrate. The invention further relates to a method of fabricating such constructions and to an apparatus for performing the method.

With the increasing miniaturisation of integrated circuit components there is now a facility to provide considerable processing power in a relatively small volume. A particularly promising development in this field has been provided by coupling a number of integrated circuits together to provide a single circuit unit constituting e.g. a computer function. One approach to this objective is to provide all the circuits in a common semiconductor wafer, the so-called wafer scale integrated circuit. Whilst this can, in principle, provide a compact and cost-effective arrangement, the introduction of the technique has been severely restricted by yield problems. This has been somewhat mitigated by the use of built-in redundancy techniques, but the wafer scale process is not yet commercially viable.

An alternative approach has been the introduction of the silicon hybrid circuit. In this arrangement a number of silicon integrated circuit chips

are disposed on a silicon substrate wafer carrying an interconnection pattern and, in some applications, further components. As the chips are tested prior to mounting on the wafer substrate, the aforementioned yield problem is overcome and there is no necessity to provide any redundancy. However, problems have been experienced in providing a reliable electrical connection between the chip and the interconnection pattern on the wafer. A preferred construction providing this interconnection is an arrangement in which the integrated circuit chips are mounted each face downwards on an array of solder bumps provided on the substrate. The solder bumps, which are disposed in register with the integrated circuit contact pads, are fused to effect the connection by heating the entire assembly to an appropriate temperature. The technique is commonly referred to as a 'flip-chip' process. Whilst the technique is well suited to mass-production methods, it suffers from the disadvantage that some of the solder connections may be imperfect resulting in a high contact resistance. As the solder joints are hidden beneath the flip-chips it is not possible, using conventional techniques, to remake a single bad joint and the only solution is to reheat the entire assembly to refuse all the solder joints. This however tends to degrade the previously good joints, thus impairing the performance of the assembly.

An object of the invention is to minimise or to overcome this disadvantage.

A further object of the invention is to provide an apparatus and method of selectively reforming soldered joints in a flip-chip hybrid assembly.

According to one aspect of the invention there is provided a method of providing a soldered

connection between a semiconductor wafer substrate and an integrated circuit mounted thereon, the method including directing focussed infra-red radiation through the wafer substrate on to the soldered connection whereby to effect fusion of that connection, the infra-red radiation having a frequency at which the substrate is transparent.

According to another aspect of the invention there is provided an apparatus for selective fusion of soldered connections between a semiconductor wafer substrate and an integrated circuit mounted thereon, the apparatus including an infra-red source operable at a frequency at which the wafer is transparent, optical means associated with the source for focussing the source output, and means for mounting an positioning said wafer with a soldered connection disposed at the focus of the infra-red source whereby the connection may be forced by radiation diverted through the wafer.

As the semiconductor wafer is transparent at the frequency of the radiation there is substantially no heating of the wafer and thus only the desired solder joint is fused. Preferably the infra-red radiation is derived from a laser, e.g. a carbon dioxide laser. Typically the semiconductor material comprises silicon.

An embodiment of the invention will now be described with reference to the accompanying drawing in which:-

Fig. 1 is a schematic view of selective soldering apparatus;

and Fig. 2 illustrates the infra-red absorption spectrum of silicon.

Referring to Fig. 1, the apparatus includes an annular mount 11 for receiving a substrate wafer 13 and for positioning the wafer relative to an infra-red source, e.g. laser 15, and its associated focussing optics 17. The mount 11 has lateral adjustment means (not shown) whereby the wafer 13 may be positioned such that a solder bump 19 on the upper wafer surface is disposed at the focal point of the laser beam. The solder bump 19 provides a means both of contacting and retaining a flip-chip 21 mounted on the wafer 13.

It will be appreciated that, when determining the focal length of the laser 15 and its associated optics 17, the refractive index of the wafer material will need to be taken into account.

The solder bond between the wafer 11 and the flip-chip 21 is formed by positioning the wafer 13 with the solder bump in register with the laser and switching the laser on for a sufficient period of time to effect fusion of the solder. The laser is then switched off and the solder is allowed to cool and solidify to complete the joint. As the heating is localised, only the selected joint is fused, the remaining solder joint of the assembly being unaffected. It is preferred to employ a tin/gold solder as no flux is required with this material.

The technique is particularly adapted to the repair or remaking of defective solder joints in a flip-chip hybrid assembly. Bad joints may be identified by electrical testing of the assembly or by examination of the assembly with an acoustic microscope . This device directs sound waves at the wafer and determines the quality of soldered joints between the wafer and the flip-chip carried thereon by analysing echoes received from the wafer.

It will be appreciated that the technique is not limited to repair applications but may also be used for device fabrication.

The optical properties of the wafer 13 determine the laser frequency range that may be employed. Specifically, the laser must have an output frequency at which the wafer is transparent. Fig. 2 illustrates the reflectivity and absorption coefficient of single crystal silicon in the infra-red region of the spectrum. As can be seen from Fig. 2, at wavelength above 1 micron the material has a low substantially constant reflectivity (R) and a low absorption coefficient (a). Consequently the material has a long absorption depth in this region of the spectrum.

Typically we employ wavelengths in the region 1 to 11 micron. In particular we have found that a carbon dioxide laser operating at 10.6 microns is suitable for providing soldered joints by the technique described herein.

The following Example illustrates the invention:

Silicon wafer substrates were prepared by providing metallisation patterns comprising either 300 A Ti/3000 A Pt/1 micron Au, or 300 A Cr/3000 A W/1 micron Au. The metallisation patterns included contact pads having dimensions in the range 25 to 50 microns square.

Integrated circuit chips were prepared by providing a contact pad metallisation comprising 300 A Ti/3000 A Pt/1 micron Su/Au flash.

The chips were mounted on the pads on the wafer and each connection was then exposed to focussed

radiation from a carbon dioxide laser to fuse the tin/gold interface so as to form a soldered joint. Soldering was carried out in an atmosphere of forming gas (90% N_2 and 10% H_2) by alloying of the tin/gold interfaces between said chip and the substrate.

The carbon dioxide laser employed to effect soldering was operated in a pulsed mode under the following conditions:-

Wavelength	10.6 microns
Pulse power	1--50 watts
Pulse length	50-500 msec.
Spot diameter	50 microns.

Subsequent electrical testing of the soldered assemblies showed that effective soldered joints has been formed.

The Example demonstrates the feasibility of the invention.

CLAIMS

1. A method of providing a soldered connection between a semiconductor wafer substrate and an integrated circuit mounted thereon, the method including directing focussed infra-red radiation through the wafer substrate on to the soldered connection whereby to effect fusion of that connection, the infra-red radiation having a frequency at which the substrate is transparent.

2. A method as claimed in claim 1 wherein the infra-red source comprises a laser.

3. A method as claimed in claim 2, wherein the source comprises a carbon dioxide laser.

4. A method as claimed in claim 3, wherein the laser is operated in a pulsed mode and has a pulse power of 10 to 50 watts.

5. A method as claimed in any one of claims 1, to 4, wherein the semiconductor comprises silicon.

6. A method as claimed in any one of claims 1 to 5, wherein the solder comprises a tin/gold alloy.

7. A method as claimed in claim 6, wherein soldering is performed in an atmosphere of forming gas.

8. A method of selective soldering substantially as described herein with reference to and as shown in the accompanying drawings.

9. An apparatus for selective fusion of soldered connections between a semiconductor wafer substrate and an integrated circuit mounted thereon, the apparatus including an infra-red source operable at a frequency at which the wafer is transparent, optical means associated with the source for focussing the source output, and means for mounting an positioning said wafer with a soldered connection disposed at the focus of the infra-red source whereby the connection may be forced by radiation directed through the wafer.

10. An apparatus as claimed in claim 9, and incorporating an acoustic microscope whereby a defective soldered connection may be identified.

11. An apparatus as claimed in claim 9 or 10, wherein said infra-red source comprises a carbon dioxide laser.

12. A selective soldering apparatus substantially as described herein with reference to and as shown in Fig. 1 of the accompanying drawings.

13. A circuit assembly manufactured or treated by a method as claims in any one of claims 1 to 8.

Published 1991 at The Patent Office, Concept House, Cardiff Road, Newport, Gwent NP9 1RH. Further copies may be obtained from Sales Branch, Unit 6, Nine Mile Point, Cwmfelinfach, Cross Keys, Newport, NP1 7HZ. Printed by Multiplex techniques ltd, St Mary Cray, Kent.